Response Under 37 C.F.R.§1.116
Expedited Procedure
Examining Group 2811

Section I. (Amendment to the Claims)

Following is a listing of claims 1-33 as amended herein, with markings to show changes made:

1. (Currently amended) A method for forming a low resistance MOSFET device comprising:

forming a gate region atop a surface of a substrate;

subsequently, forming source and drain extension regions in the substrate, wherein a channel region is formed between said source and drain extension regions in the substrate;

subsequently, forming first spacers each having a first spacer width on sidewalls of said gate region;

subsequently, forming source and drain regions in the substrate abutting the source and drain extension regions, respectively;

subsequently, forming first silicide regions each having a first vertical silicide thickness in said substrate, wherein the first vertical silicide thickness is from about 2 to about 15 nm;

subsequently, forming second spacers atop said substrate each having a second spacer width along sidewalls of the first spacers, wherein said second spacers protect said first silicide regions in said substrate; and

subsequently, forming second silicide regions in said substrate, wherein said second silicide regions each have a second vertical silicide thickness that is greater than said first vertical silicide thickness~~, and wherein the first vertical silicide thickness is from about 2 to about 15 nm~~.

2. (Original) The method of Claim 1 wherein said forming of said gate region further comprises predoping of said gate region.

3. (Original) The method of Claim 2 wherein said predoping is performed by ion implantation of a type III-A element or a type V element into said gate region.

4. (Original) The method of Claim 3 where predoping is achieved via ion implantation of phosphorus into said gate region.

5. (Cancelled)

6. (Previously presented) The method of Claim 1 wherein said first spacers width is from about 5 nm to about 20 nm.

7. (Previously presented) The method of Claim 1 wherein said first spacers width is from about 7 nm to about 15 nm.

8. (Original) The method of Claim 1 wherein said second spacers width is from about 20 nm to about 90 nm.

9. (Original) The method of Claim 1 wherein said second spacers width is from about 30 nm to about 70 nm.

10-11. (Cancelled)

12. (Presently presented) The method of Claim 1 wherein said forming of said first silicide regions comprises depositing a first metal layer upon an exposed surface of said substrate and annealing.

13. (Original) The method of Claim 12 where said first metal layer has a thickness from about 2 nm to about 7 nm.

14. (Original) The method of Claim 13 where said first metal layer comprises Ta, Ti, W, Pt, Co, Ni, or combinations thereof.

15-16. (Cancelled)

17. (Previously presented) The method of Claim 1 wherein said first vertical silicide thickness is from about 5 nm to about 12 nm.

18. (Currently amended) The method of Claim 1 ~~wherein said first silicide regions is formed in said substrate having a channel region beneath said gate region~~, where the distance between said first silicide regions and said channel region is from about 2 nm to about 15 nm.

19. (Currently amended) The method of Claim 1 ~~wherein said first silicide regions is formed in said substrate having a channel region beneath said gate region~~, where the distance between said first silicide regions and said channel region is from about 3 nm to about 10 nm.

20-33. (Cancelled)